REMARKS

The Examiner is again thanked for the thorough examination of the present application. Independent Claims 5, 11, 17, 20 and 22 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found beginning on pages 11-13 of the originally filed specification, for example. No new matter is being added.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a computer system. As recited in amended independent Claim 5, for example, the computer system includes a master apparatus and a slave apparatus for communicating therewith via a universal serial bus (USB) protocol. The slave apparatus includes a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon, and for acknowledging and recording a new message only when a transfer interruption signal is not supplied. Moreover, a plurality of state latches and control circuitry cooperating therewith receive the status signals from the sending/receiving circuit and supply state signals of the sending/receiving circuit based thereon. The slave apparatus further includes a microprocessor for processing applications of the slave apparatus

and also for processing the binary information received by the sending/receiving circuit. Furthermore, an interruption state latch and a control circuit cooperating therewith supply an interruption signal to the microprocessor once the end of a message has been acknowledged and supply the transfer interruption signal to the microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor interruption signal is supplied.

As such, the slave apparatus in accordance with the present invention may advantageously allow, at the end of a message, an acceptance of the start of a following message while the microprocessor is unavailable, without the need for re-sending the start of the message. Independent Claim 11 is directed to a similar computer system, independent Claim 17 is directed to a similar slave apparatus, and independent Claims 20 and 22 are directed to related methods. Each of these claims has been amended to recite that the sending/receiving circuit acknowledges and records a new message only when a transfer interruption signal is not supplied, that the interruption signal is supplied once the end of a message has been acknowledged, and that the transfer interruption signal is supplied to the microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor interruption signal is supplied, similar to Claim 5.

II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 11, 17, 20 and 22 over the prior art discussed in the background of the present application (the "admitted prior art") in view of Saito et al. (U.S. Patent No. 5,019,966). The admitted prior art describes a typical master-slave computer system arrangement, such as the one illustrated in FIG. 1 of the present application. Beginning on page 2, line 29, it is noted that during different transfer stages between the master apparatus and the slave apparatus, there are provisions which allow the master apparatus to repeat its part of the message IN and OUT while the microcontroller (i.e., microprocessor) of the slave apparatus is unavailable. If the phase that follows is a start phase and its microcontroller is unavailable, the slave apparatus returns no signal (no NAK, nor STALL, nor ACK signal), which is interpreted by the master apparatus as a transmission error. In such case the master apparatus resends the message.

Such an operation only appears if the time period during which the slave microcontroller is unavailable exceeds a time interval separating two consecutive messages. However, in high-speed data transfers, these time intervals between two messages are increasingly short. Yet, the microcontroller of the slave apparatus has to perform more and more tasks, while the time periods during which it is unavailable are longer and longer.

At the end of the transfer stages, an interruption of the microcontroller to process the part of the transmitted

message may be requested. To this end, a flag CTR is set to the logic 1 state to indicate that an interruption is requested (see FIG. 3(d) of the present application). After a certain time (which depends on the application), the interruption requested by the USB bus is processed. At the end of the interruption, the program executed by the microcontroller returns the flag CTR to the logic 0 state, thus authorizing the transfer of the following part of the message. A software state machine then processes the information concerning the event of the USB message extracted by the interruption routine.

As a result of the above operations, no transfer over the USB bus is authorized when the flag is in the logic 1 state. There is, therefore, a dependency between the time for processing an interruption and the time delay in accepting the following transfer, the time for processing the interruption being linked to the microcontroller's operating frequency. Further, the time delay between each transaction depends on the master apparatus in that if that time delay is shorter than the minimum time for processing an interruption by the microcontroller, the following transfer cannot be authorized. This can result in the failure of the transaction.

The Examiner correctly acknowledges that the admitted prior art fails to teach or fairly suggest that the interruption signal has been recorded by the sending/receiving circuit when the microprocessor is unavailable. However, the Examiner contends that Saito et al. provides this noted deficiency. Saito et al. is directed to a data processing system which includes a data processing unit for supplying a predetermined length of data to be transferred and generating a transfer start signal. The system

further includes a data transferring unit receiving the predetermined length of data from the data processing unit and for transferring the predetermined length of data in a serial form to a receiving data processor. The transmitting data processor also includes a busy detector for detecting a busy signal from the receiving data processor, a register for temporarily holding the transfer start signal from the data processing unit, and a start controller associated with the data transferring unit. The start controller is for causing the data transferring unit to stop the transfer of data during the period the busy signal is active, and for allowing the data transferring unit to start the transfer of data when the busy signal becomes inactive after the transfer start signal is generated.

The above-noted independent claims have been amended to recite that the sending/receiving circuit acknowledges and records a new message only when a transfer interruption signal is not supplied, that the interruption signal is supplied once the end of a message has been acknowledged, and that the transfer interruption signal is supplied to the microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor interruption signal is supplied. It is respectfully submitted that the selective combination of references fails to teach or fairly suggest all of the recitations of the above-noted independent claims as amended.

In the Saito et al. system, when a data transfer is attempted from a transmitting data processor **100** to a receiving data processor **310**, the receiving data processor stores serial data transferred from the transmitting data processor in a shift

register and then generates an interrupt signal. The stored data is then read out of the shift register and processing thereon begins. Concurrently, a busy signal is generated on a busy signal line connected to the transmitting data processor, which informs the transmitting data processor that the receiving data processor is busy and inhibits further transmissions until the busy signal is removed. See, e.g., FIG. 1 and col. 6, lines 9-17 of Saito et al.

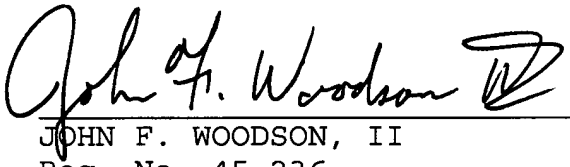
In sharp contrast, the above-noted independent claims recite that the sending/receiving circuit acknowledges and records a new message only when a transfer interruption signal is not supplied thereto. Yet, the receiving data processor of Saito et al. receives and stores in the shift register thereof any received data. This is because the receiving data processor generates a busy signal for the transmitting data processor, which prohibits it from transmitting further data while the receiving data processor is busy. Thus, the receiving data processor is not supplied with any interruption signal that prevents it from recording or acknowledging a new message, nor does it need any such interruption signal since it is controlling the transmitting data processor. As such, Saito et al. teaches away from the claimed combination.

Accordingly, since none of the prior art of record teaches or fairly suggests all of the features recited in independent Claims 5, 11, 17, 20 and 22, it is respectfully submitted that these claims are patentable. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



JOHN F. WOODSON, II
Reg. No. 45,236
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
Telephone: 407/841-2330
Fax: 407/841-2343
Attorney for Applicants

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CERTIFICATE OF MAILING

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